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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,440	11/19/2003	Monier Maher	NVDA/JAG-08-0114-US	3945
26290 7590 06/23/2010 PATTERSON & SHERIDAN, L.L.P. 3040 POST OAK BOULEVARD SUITE 1500 HOUSTON, TX 77056				
EXAMINER				
BAHTA, KIDEST				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/715,440

**Applicant(s)**

MAHER ET AL.

**Examiner**

KIDEST BAHTA

**Art Unit**

2123

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 May 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,4-12 and 16-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4-12 and 16-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB-08)  
Paper No(s)/Mail Date 5/5/10, 3/3/10
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. The amendment filed on 5/17/10 has been received and fully considered; claims 1, 4-12, 16-28 are presented for examination. Claims 2-3, and 13-15 are cancelled.
2. Regarding the objected abstract withdraws since applicant amends the abstract. The new abstract is accepted.

***Response to Arguments***

3. Applicant's arguments with respect to claims 1, 4-12, and 17-28 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4-12 and 16-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook et al. (US 6,342,892) in view of Suzuoki et al. (US 6526491).

Regarding claims 1 and 9 Suzoki discloses,

A dedicated, hardware-based Physics Processing Unit (PPU), comprising: a vector processor (element 303, 305, 307) adapted to perform multiple, parallel floating point operations to generate physics data (Fig. 4); and a data communication circuit adapted to communicate the physics data to a host (,Fig. 3)

Vanhook fails to disclose a PPU Control Engine (PCE) receiving commands from the CPU and controlling communication the physics data from the PPU to the host; an external memory and an internal memory and a Data Movement Engine (DME) controlling the movement of data between the external memory and the internal memory in response to instructions received from the PCE.

Suzuoki discloses a PPU Control Engine (PCE) receiving commands from the CPU and controlling communication the physics data from the PPU to the host; an external memory and an internal memory (Fig. 2, element 225); and a Data Movement Engine (DME) controlling the movement of data between the external memory and the internal memory in response to instructions received from the PCE (Fig. 8, element 810; 1206, Fig. 12A).

It would have been obvious to a person of ordinary skill in the art at the time of invention was made to modify the teachings of Van Hook with the teachings of Suzuoki in order to balancing the memory access and floating-point calculations.

Regarding claims 4-8, 10-12, and 16-28, Van Hook discloses,

4. The PPU of claim 3, further comprising: a Floating Point Engine (FPE) performing multiple, parallel floating point operations on data stored in the internal memory (column 18, lines 8-11).
5. The PPU of claim 4, wherein the internal memory is operatively connected to the DME, and further comprising: a high-speed memory bus operatively connecting an external high-speed memory to at least one of the DME and the FPE (column 22, lines 13-15; column 17, lines 17-19; column 18, lines 8-11).
6. The PPU of claim 5, wherein the internal memory comprises multiple banks allowing multiple data threading operations (column 19, lines 41-50).
7. The PPU of claim 3, wherein the PCE comprises control and communication software stored in a RISC core (column 19, lines 60-67).
8. The PPU of claim 5, wherein the internal memory comprises first and second banks, and wherein the DME further comprises: a first unidirectional crossbar connected to the first bank (column 2, lines 15-39); a second unidirectional crossbar connected to the second bank (column 2, lines 15-39); and, a bi-directional crossbar connecting first and second crossbars to the external high-speed memory (column 4, lines 14-22).

10. The PPU of claim 9, wherein the system comprises a Personal Computer (PC); and wherein the PPU comprises an expansion board adapted for incorporation within the PC, the expansion board mounting the ASIC and the external memory (column 13, lines 13-16).

11. The PPU of claim 10, further comprising circuitry enabling at least one data communications protocol between the PPU and CPU (Fig. 2).

16. The PPU of claim 15, wherein the internal memory is operatively connected to the DME, and further comprising: a high-speed memory bus operatively connecting the external memory to at least one of the DME and the FPE (Fig. 5, column 18, lines 8-11).

17. The PPU of claim 16, wherein the internal memory comprises multiple banks allowing multiple data threading operations (Fig. 5).

18. The PPU of claim 17, wherein the internal memory further comprises: an Inter-Engine memory transferring data between the DME and FPE (column 19, lines 60-67).

19. The PPU of claim 18, wherein the internal memory further comprises: a Scratch Pad memory (Fig. 6; column 19, lines 41-50).

20. The PPU of claim 14, further comprising a command packet queue transferring

command packets from the PCE to the DME (column 19, lines 61-67; column 20, lines 1-8).

21. The PPU of claim 15, wherein the FPE comprises a plurality of Vector Floating-point Units (column 18, lines 8-11).

22. The PPU of claim 21, wherein at least one of the command packets defines a vector length of variable length (column 8, lines 39-46).

23. The PPU of claim 15, wherein the DME comprises a plurality of Memory Control Units (MCUs) and a Switch Fabric connecting the MCUs to the external memory (Fig. 5); and, wherein the FPE comprises a plurality of Vector Processing Engines (VPEs) receiving data from at least one of the MCUs via a VPE bus (.

24. The PPU of claim 23, wherein each Vector Processing Engine (VPE) comprises a plurality of Vector Processing Units (VPUs) receiving data from the VPE bus (column 17, lines 30-42).

25. The PPU of claim 24, wherein each VPU comprises: a dual bank Inter-Engine Memory (IEM) receiving data from the VPE bus (column 19, lines 61-67); one or more data registers receiving data from the IEM under the control of an associated Load/Store Unit; and an Execution Unit performing parallel floating point operations

(column 2, lines 15-39, column 4, lines 14-22).

26. The PPU of claim 23, wherein at least one command packet received from the PCE defines a vector length of variable length (column 8, lines 39-46).

27. The PPU of claim 23, wherein the Switch Fabric comprises at least one crossbar circuit (column 2, lines 15-39, column 4, lines 14-22).

28. The PPU of claim 24, wherein each VPU is dynamically re-configurable (element 420).

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook, and Suzuki, as applied to claims 9-11 above, in view of Intel (Intel PCI and PCI Express; note that the subject matter relied upon in the reference is dated).

Claim 12, Van Hook does not disclose that the CPU and PPU communicate via at least one selected from a group of physical interfaces consisting of: USB, USB2, Firewire, PCI, PCI-X, PCI-Express, and Ethernet. On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI- Express interface (pages 2-3, PCI, PCI Express). The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the PCI-



Express interface supports important features such as power management and the ability to handle both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and Van Hook and Suzuki as modified that there exists a bus that connects the CPU and the PPU.

### ***Double Patenting***

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 4-12, and 16-28 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7, 10-17 and 25-40 of copending Application No. 10/715,459 and unpatentable over claims 1, 5-19, 26-35 of copending Application No. 10/839,155. Although the conflicting claims are not identical, they are not patentably distinct from each other because they disclose the same subject matters.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kidest Bahta whose telephone number is 571-272-3737.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you

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have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kideest Bahta/

Primary Examiner, Art Unit 2123